ALLEGRO CL® @Work!

A Franz Inc. Customer Success Story

Cadence Design Systems, Inc.

Design Planner Tool Suite for ASIC Floor-Planning Design

Cadence Design Systems, a world-renowned provider of EDA software, selected Allegro CL as the tool of choice for developing the company's front-end tool suite, Design Planner (DP). Cadence takes advantage of Allegro CL's ANSI-standard Common Lisp to give them maximum dynamic behavior for on-demand customization of their software in a rapidly changing environment.

"DP is the cockpit area," says Mark Bales, R & D Fellow, "from which the design can interact with the entire system. From DP, we can fire off the design to any of the other tools required. We can shoot it off to the timing analysis programs, placers, routers, clock-tree generators, etc. It's the place from where we can direct the whole design."

Design Planner comprises three products, Top-Down DP, Logic DP, and Physical DP. All three contribute to the end-result of creating an IC (chip) floor plan.

Top-Down DP

Top-Down DP begins the initial phase of the floor plan design, allowing the user to start accounting for the physical floor plan even during the early phases of behavioral design using a hardware description language. Following Logic Synthesis, the program then estimates how many gates will be generated, partitions the design, and begins to get a read on interconnect delays. "Interconnect delays become important in Deep-submicron design," says Bales. "They have a huge impact on the eventual performance [speed] of the chip. By using DP, you can begin estimating these delays way back when designing the chip at a behavioral level."

Logic DP

Logic DP starts with the gate level net list obtained from Top-Down DP and ends at the

> **"Because of these dynamic features, we can quickly change our app to whatever degree our customers need, or do an easy patch and get them back up and running."**
>
> *Mark Bales, Fellow R&D*

point where real placement occurs. In the logic design phase, the designer is able to obtain highly accurate estimates of interconnect delays and the resulting performance.

These estimates are accomplished through complex algorithms which provide automatic logic grouping and physical partitioning that analyze a logic hierarchy. They also determine which portions of the hierarchy are structured for problem-free physical implementation; and which are unstructured and must be processed further to avoid routability problems. Automatic physical partitioning and regrouping algorithms are then used on the unstructured logic to repartition the design for optimum physical implementation. The results are increased accuracy of size and performance estimates and reduced number and length of iterations.

Physical DP

Physical DP begins with the full placement obtained with Logic DP and ends with the full routing of cells and thereby full routing of the circuit. At this stage, the circuit is completely wired. Once the design has progressed through Physical DP, the designer can use additional Cadence tools to precisely verify the interconnect delays using the actual wiring of the circuit. "If the design process is not done properly," says Bales, " there is real danger that the chip will not run at the speed it is supposed to." Unlike similar design tools which make only relatively simple calculations early in the design process, DP gains a closely accurate estimate of interconnect delays considerably before the circuit is wired. These estimates are continually refined as the implementation of the design continues and more information about the design is known. Consequently, designers avoid costly surprises after the chip is completed and expected to perform at speed.

"The faster the clock speed, the harder it is to design," says Bales. "That's why using the DP approach as opposed to other tools which use only flat placement and routing is so critical." The Design Planner suite is a hierarchical method of chip design that breaks down the whole into individual portions where a problem can be solved in each piece of the puzzle. "The difference between the two approaches can be likened to making a quilt," continues Bales. The DP method is like a group of people all working different parts of the quilt to make the whole. Systems that use only flat placement and routing are trying to perform the unwieldy task of having a single person sew a immense quilt entirely alone."

Allegro CL Critical to On-the-Fly Customization

"We chose Allegro CL," says Bales, "because Lisp is dynamic and easy to modify and update. We often get specific requests from customers for particular customizations or someone will bring us a design that we've never seen before. Because of these dynamic features, we can quickly change our app to whatever degree our customers need or do an easy patch and get them back up and running. It's also an excellent choice for tool flows that control commands and how the system is used." Cadence has set up the DP system so that all their menus and dialogs drive Lisp. This is beneficial, Bales explains, "so that if you need to extend it, it is easy to do. It makes for a simpler interface when something needs to be modified. As far as the ability to combine features and functionality and create new features and functionality as well as running moderate to complex algorithms, the Allegro CL development environment is unparalleled."

For more information about Cadence Design Systems, Inc., you may visit their web site at www.cadence.com.